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4	1	((memory or storage) adj location)) and wavelet	EPO; JPO	2004/03/08 07:16
5	0	((memory or storage) adj location)) and lead\$4 and trail\$4	EPO; JPO	2004/03/08 07:17
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5	174	708/203.ccls.	USPAT; DERWENT	2004/03/08 07:37
6	13	708/203.ccls. and wavelet	USPAT; DERWENT	2004/03/08 07:37
8	1	((708/203.ccls. and wavelet) and ((memory or storage) near (location or address))) and leading and trailing	USPAT; DERWENT	2004/03/08 07:40
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	U	1	Document ID	Issue Date	Page s	Title	Current OR
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2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5745392 A	19980428	32	Method for reducing data storage and transmission requirements for seismic data	708/203
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Last Name = TERA0

First Name = NORIYUKI

Application#	Patent#	Status	Date Filed	Title	Inventor Name 6
09549511	Not Issued	030	04/14/2000	METHOD AND APPARATUS FOR HIGH SPEED DATA COMPRESSION AND DECOMPRESSION	TERAO, NORIYUKI
08082371	5408113	150	06/28/1993	HIGH SENSITIVITY IMPROVED PHOTOELECTRIC IMAGING DEVICE WITH A HIGH SIGNAL TO NOISE RATIO	TERAO , NORIYUKI
08078409	5316960	150	06/17/1993	C-MOS THIN FILM TRANSISTOR DEVICE MANUFACTURING METHOD	TERAO , NORIYUKI
07824552	Not Issued	161	01/23/1992	C-MOS THIN FILM TRANSISTOR DEVICE AND MANUFACTURING METHOD THEREOF	TERAO , NORIYUKI
07550154	Not Issued	161	07/09/1990	C-MOS THIN FILM TRANSISTOR DEVICE AND MANUFACTURING METHOD THEREOF	TERAO , NORIYUKI
07451176	5027382	150	12/15/1989	SHIFT REGISTER CIRCUIT	TERAO , NORIYUKI

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Instrumentation and Measurement, IEEE Transactions on , Volume: 38 , Issue: 1 , Feb. 1989

Pages: 64 - 73

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1 Line-based, reduced memory, wavelet image compression
Chrysafis, C.; Ortega, A.;

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2 Hardware implementation of a wavelet based image compression coder
Singh, J.; Antoniou, A.; Shpak, D.J.;

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Pentland, A.P.;

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4 TSA-tree: a wavelet-based approach to improve the efficiency of multi-level surprise and trend queries on time-series data

Shahabi, C.; Tian, X.; Zhao, W.;

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Huang Xianfeng; Chen Yunping;

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8 Optimal memory organization for scalable texture codecs in MPEG-4

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Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 9 , Issue: 2 , March 1999

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10 Synthesis of minimum-area folded architectures for rectangular multidimensional multirate DSP systems

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David Chan Tat Wai; Xia Yibin;

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13 A neural-fuzzy classifier for recognition of power quality disturbances

Jiansheng Huang; Negnevitsky, M.; Nguyen, D.T.;

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14 Synthesis of folded pipelined architectures for multirate

DSP algorithms*Denk, T.C.; Parhi, K.K.;*

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15 Optical pattern recognition: architectures and techniques*Yu, F.T.S.; Gregory, D.A.;*

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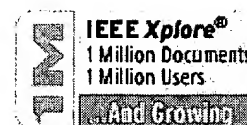
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17 **A VLSI architecture of spatial combinative lifting algorithm based 2-D DWT/IDWT**

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